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HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
DUONG, FRANK	

ART UNIT	PAPER NUMBER
2666	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,961	NOWELL ET AL.	
	Examiner	Art Unit	
	Frank Duong	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the amendment and Declaration Under CFR § 1.131 dated 1/15/2004. Claims 1-44 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujimoto et al (Skew-Free Parallel Optical Transmission Systems, IEEE, pages 1822-1831, October 1998) (hereinafter "Fujimoto").

Regarding **claim 1**, in accordance Fujimoto reference entirety, Fujimoto discloses a system (Figures 2, 5, 10 and 11) for transferring synchronous optical network/synchronous digital hierarchy (SONET/SDH) frames (156 Mb/s) (*see page 1822, right column, Fujimoto discloses basic bit rate of SDH is 156 Mb/s*) between a first and second node (*Figure 2 or 5; TX and RX or Transmitter Module and Receiver Module and Figures 10-11; Coder LSI and Decoder LSI*) comprising:

a demultiplexer (*page 1827, Figure 10; P/S*) to map SONET/SDH frames (156 Mb/s) onto a plurality of data channels (Ch1-Ch5) (*see Figures 10 and 11 and the corresponding description*);

an encoder (*page 1827, Figure 10*) to encode and translate data onto each data channel for transmission (*Coder LSI*);

a decoder (*page 1827, Figure 11*) to decode and translate data on each data channel for reception (*Decoder LSI*); and

a multiplexer (*page 1827, Figure 10; S/P*) to map the plurality of data channels (Ch1-Ch5) onto SONET/SDH frames (156 Mb/s) (*see Figures 10 and 11 and the corresponding description*).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Fujimoto further discloses wherein the multiplexer includes a framer (*Figure 10; F/C INS*) to determine the position of frame markers in the data (*see page 1826, left column, section A*).

Regarding **claim 3**, in addition to features recited in base claim 1 (see rationales discussed above), Fujimoto further discloses wherein the first and second nodes communicate over parallel transmission links (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link).

Regarding **claim 4**, in addition to features recited in base claim 2 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission links comprise a parallel-optics based transmission link (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link).

Regarding **claim 5**, in addition to features recited in base claim 3 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission link

comprise a wavelength division multiplex (WDM) based transmission link (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link).

Regarding **claim 6**, in accordance Fujimoto reference entirety, Fujimoto discloses a method (*Figures 2, 5, 10 and 11*) for transferring synchronous optical network/synchronous digital hierarchy (SONET/SDH) frames between a first and second node *Figure 2 or 5; TX and RX or Transmitter Module and Receiver Module and Figures 10-11; Coder LSI and Decoder LSI*) comprising:

mapping (Figure 10) the SONET/SDH frames (156 Mb/s) onto a plurality of data channels (Ch1-Ch5) (see Figure 10 and description on page 1826, left column, section A pertaining Figure 10); and

transferring (Figure 10) the SONET/SDH frames (156 Mb/s) over a plurality of parallel transmission links (Ch1-Ch5) (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link) (see Figure 10 and description on page 1826, left column, section A pertaining Figure 10)

Regarding **claim 7**, in addition to features recited in base claim 6 (see rationales discussed above), Fujimoto further discloses wherein transferring the SONET/SDH frames (156 Mb/s) over parallel transmission links includes transmitting (TX Module or Coder LSI) and receiving (RX Module or Decoder LSI) the SONET/SDH frames over parallel transmission links (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link).

Regarding **claim 8**, in addition to features recited in base claim 7 (see rationales discussed above), Fujimoto further discloses byte stripping of the SONET/SDH frames

onto parallel data channels (see Figure 10 and the description pertaining SWAP circuit disclosed on page 1826, left column).

Regarding **claim 9**, in addition to features recited in base claim 7 (see rationales discussed above), Fujimoto further discloses encoding each data channel for data formatting (see Figure 10).

Regarding **claim 10**, in addition to features recited in base claim 7 (see rationales discussed above), Fujimoto further discloses framing each data channel (*see Figure 10; element F/C INS*).

Regarding **claims 11-12**, in addition to features recited in base claim 6 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission link comprises a 12 fiber (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link).

Regarding **claim 13**, in addition to features recited in base claim 6 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission link comprises a wavelength division multiplex (WDM) based transmission link (see Figure 5; ribbon fiber or Figures 10-11; parallel optical link).

Regarding **claim 14**, in addition to features recited in base claim 6 (see rationales discussed above), Fujimoto further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*see page 1830, right column; CONCLUSION, Fujimoto discloses the proposed multiplexing-based line code mB1A and non-multiplexing-based line code are for future Gbit/s interconnection. Thus, it is inherent that OC-192/STM-64 line rate is included in the recited statement*).

Regarding **claim 15**, in addition to features recited in base claim 7 (see rationales discussed above), Fujimoto further discloses wherein receiving SONET/SDH frames further comprises, receiving (Figure 11) data from each of the parallel transmission links (Ch1-Ch5); decoding each data channel (*Figure 11*); realigning each data channel to compensate for an inter-channel skew (Figure 11; element SSC); and recombining (S/P) the data channels into a SONET/SDH frame (156 Mb/s).

Regarding **claim 16**, in accordance Fujimoto reference entirety, Fujimoto discloses a method (*Figures 2, 5 and 10-11*) for transferring synchronous optical network (SONET)/synchronous digital hierarchy (SDH) frames (*see page 1822, right column, Fujimoto discloses basic bit rate of SDH is 156 Mb/s*) over a parallel transmission system (*Figure 5; Fiber Ribbon*) comprising:

mapping (Figure 10; P/S) SONET/SDH frames (*156 Mb/s*) onto data channels (Ch1-Ch5); and

transmitting (F/C INS output) the SONET/SDH frames over a plurality of parallel transmission links (*Ch1-Ch5*).

Regarding **claim 17**, in accordance Fujimoto reference entirety, Fujimoto discloses a method (*Figures 2, 5 and 10-11*) of transmitting SONET/SDH frames (*see page 1822, right column, Fujimoto discloses basic bit rate of SDH is 156 Mb/s*) having framer markers (*F/C INS*), the method comprising:

determining the position of the frame markers (*see page 1826, left column; F/C INS*);

byte stripping of the SONET/SDH frames (*P/S*) onto a plurality of parallel of data channels (*Ch1-Ch5*) (see page 1826, left column);

encoding (Figure 10) each data channel (see page 1826, left column); and

transmitting (F/C INS output) the channels over parallel transmission links (*Ch1-CH5*).

Regarding **claims 18-19**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission link comprises a 12 fiber (*Figure 5; Fiber Ribbon*).

Regarding **claim 20**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission links comprises a wavelength division multiplex (WDM) based transmission link (*Figure 5; Fiber Ribbon*).

Regarding **claim 21**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*see page 1830, right column; CONCLUSION, Fujimoto discloses the proposed multiplexing-based line code mB1A and non-multiplexing-based line code are for future Gbit/s interconnection. Thus, it is inherent that OC-192/STM-64 line rate is included in the recited statement*).

Regarding **claim 22**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein frame delimiting is performed by overwriting at least a SONET byte on each data channel (*see page 4,*

second paragraph, "some SONET framing bytes on each data channel are overwritten with a frame delimiter").

Regarding **claim 23**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein at least a first three SONET framing bytes are overwritten on each data channel (see page 1826, left column pertaining F/C INS).

Regarding **claim 24**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein unique frame delimiters are used on a subset of the data channels (see page 1826, left column pertaining F/C INS).

Regarding **claim 25**, in addition to features recited in base claim 24 (see rationales discussed above), Fujimoto further discloses wherein a first, frame delimiter is used for a first half of the data channel and a second frame delimiter is used for a second half of the data channels (see page 1826, left column pertaining F/C INS).

Regarding **claim 26**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein each channel is encoded using a block-code (Figure 10).

Regarding **claim 27**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein the data channels are logically combined in such a manner to enable recovery of a single data channel and the logically combined channel exists as a separate data channel (*see Figure 11; S/P*).

Regarding **claim 28**, in addition to features recited in base claim 17 (see rationales discussed above), Fujimoto further discloses wherein a further data channel carries cyclic redundancy check (CRC) bits for the plurality of data channels (*see page 1827, left column pertaining SCR circuit*).

Regarding **claim 29**, in accordance Fujimoto reference entirety, Fujimoto discloses a method (*Figure 11 and description on page 1826, left column*) of receiving SONET/SDH frames (*156 Mb/s*) over a parallel transmission system (*Figure 11*) comprising:

recovering (SDCR) data from each transmission link (Ch1-Ch5);

decoding (Figure 11) each data channel (*Ch1-Ch5*);

realigning (SSC) each data channel to compensate for an inter-channel skew (; and

recombining (S/P) the data channels (Ch1-Ch5) into a SONET/SDH frame (156 Mb/s).

Regarding **claims 30-31**, in addition to features recited in base claim 29 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission link comprises a 12 fiber (Figure 5; ribbon fiber).

Regarding **claim 32**, in addition to features recited in base claim 29 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission links comprises a wavelength division multiplex (WDM) based transmission link (Figure 5; ribbon fiber).

Regarding **claim 33**, in addition to features recited in base claim 29 (see rationales discussed above), Fujimoto further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*see page 1830, right column; CONCLUSION, Fujimoto discloses the proposed multiplexing-based line code mB1A and non-multiplexing-based line code are for future Gbit/s interconnection. Thus, it is inherent that OC-192/STM-64 line rate is included in the recited statement*).

Regarding **claim 34**, in addition to features recited in base claim 29 (see rationales discussed above), Fujimoto further discloses wherein the receiver detects a polarity of the transmission links by use of unique frame delimiters on subset of the data channels (*see page 1826, left column pertaining the SSC circuit*).

Regarding **claim 35**, in addition to features recited in base claim 30 (see rationales discussed above), Fujimoto further discloses a loss of synchronization condition on a channel if a plurality of code word violation occurs (*see page 1826, right column pertaining Parallel Reframing system*).

Regarding **claim 36**, in addition to features recited in base claim 29 (see rationales discussed above), Fujimoto further discloses wherein a channel failure is detected using the loss of synchronization condition (*see page 1826, right column pertaining Parallel Reframing system*).

Regarding **claim 37**, in addition to features recited in base claim 29 (see rationales discussed above), Fujimoto further discloses detecting and correcting errors on the data channels by calculating a cyclic redundancy check for a block of data on the data channel; comparing it to a corresponding, separately-transmitted CRC for the

block; and recovering the data from a protection channel if the CRC's do not match (*see page 1826, right column pertaining Parallel Reframing system*).

Regarding **claim 38**, in accordance Fujimoto reference entirety, Fujimoto discloses a transceiver module (*Figures 2, 5 and 10-11*) for transferring SONET/SDH frames (*156 Mb/s*) between a first and second node (TX Module and Rx Module), comprising:

a converter circuit (*Figure 15; Coder*) to adapt incoming signals (156 Mb/s) for transmission of parallel (*fiber ribbon*);

a parallel transmit optic module (*LD/CPL*) to transmit data channels (*Ch1-Ch5*); and

a parallel receive optic module (*PD/CPL*) to receive data channels (*Ch1-Ch5*).

Regarding **claim 39**, in addition to features recited in base claim 38 (see rationales discussed above), Fujimoto further discloses wherein a rate for transferring SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*see page 1830, right column; CONCLUSION, Fujimoto discloses the proposed multiplexing-based line code mB1A and non-multiplexing-based line code are for future Gbit/s interconnection. Thus, it is inherent that OC-192/STM-64 line rate is included in the recited statement*).

Regarding **claim 40**, in addition to features recited in base claim 38 (see rationales discussed above), Fujimoto further discloses wherein the first and second node communicate over parallel transmission links (*Fiber Ribbon*).

Regarding **claim 41**, in addition to features recited in base claim 40 (see rationales discussed above), Fujimoto further discloses wherein the parallel

transmission links (*Fiber Ribbon*) comprises a parallel-optics based transmission link (*Fiber Ribbon*).

Regarding **claim 42**, in addition to features recited in base claim 40 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmission links comprises a wavelength division multiplex (WDM) based transmission link (*Fiber Ribbon*).

Regarding **claim 43**, in addition to features recited in base claim 38 (see rationales discussed above), Fujimoto further discloses wherein the converter circuit interfaces with a frame chip (*see Figure 5; Transmitter Module*).

Regarding **claim 44**, in addition to features recited in base claim 38 (see rationales discussed above), Fujimoto further discloses wherein the parallel transmit optic module is integral with the parallel receive optic module (*see Figure 5*).

Response to Arguments

3. Applicant's arguments in view of CFR § 1.132, see page 8 of the response, filed 1/15/04, with respect to rejection have been fully considered and are persuasive. The rejection of claims 1-44 has been withdrawn.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ducaroir et al (USP 6,167,077).

Finney et al (USP 5,570,356).

Shimada et al, GaAs 10 Gb/s 64:1 Multiplexer/Demultiplexer Chip Sets, IEEE, pages 503-511, April 1996.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is (703) 308-5428. The examiner can normally be reached on 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (703) 308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Frank Duong
Examiner
Art Unit 2666

March 29, 2004